

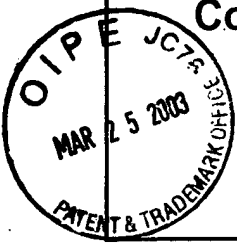
RCE/2815#

PTO/SB/30 (08-00)

Approved for use through 10/31/2002. OMB 0651-0031

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Request for Continued Examination (RCE) Transmittal

Address to:
Commissioner for Patents
BOX RCE
Washington, DC 20231

Application Number	09/939,752
Filing Date	August 28, 2001
First Named Inventor	Masaki KOMAKI
Group Art Unit	2815
Examiner Name	J. Nguyen
Attorney Docket Number	024016-00014

This is a Request for Continued Examination (RCE) under 37 C.F.R. § 1.114 of the above identified application. Request for Continued Examination (RCE) practice under 37 CFR 1.114 does not apply to any utility or plant application filed prior to June 8, 1995, or to any design application. See instruction Sheet for RCEs (not to be submitted to the USPTO) page 2

1. Submission required under 37 CFR § 1.114

- a. ☐ Previously submitted
 - i. ☐ Consider the amendment(s)/reply under 37 CFR 1.116 previously filed on _____. (Any unentered amendment(s) referred to above will be entered).
 - ii. ☐ Consider the arguments in the Appeal Brief or Reply Brief previously filed on ____.
 - iii. ☐ Other _____
- b. ☒ Enclosed
 - i. ☒ Amendment/Reply
 - ii. ☐ Affidavit(s)/Declaration(s)
 - iii. ☐ Information Disclosure Statement (IDS)
 - vi. ☐ Other _____

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01 FC:1801
02 FC:1202
03 FC:1201

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2. Miscellaneous

- a. ☐ Suspension of action on the above-identified application is requested under 37 CFR 1.103(c) for a period of __ months. (Period of suspension shall not exceed 3 months; Fee under 37 CFR 1.17(i) required)
- b. ☐ Other _____

3. Fees

The RCE fee under 37 CFR 1.17(e) is required by 37 CFR 1.114 when the RCE is filed.

- a. ☒ The Director is authorized to charge any deficiency fees, or credit any overpayments, to Deposit Account No. 01-2300.
 - i. ☐ RCE fee required under 37 CFR 1.17(e)
 - ii. ☐ Extension of time fee (37 CFR 1.136 and 1.17)
 - iii. ☐ Other _____
- b. ☒ A check in the amount of \$ 1,064.00 (\$750.00 to cover the official RCE filing fee, \$204.00 for the extra claim fee, and \$110.00 to cover the extension of time) is enclosed.
- c. ☐ Payment by credit card (Form PTO-2038 enclosed)

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED

Name (Print Type)	Raymond J. Ho	Registration No. (Attorney/Agent)	41,838
Signature		Date	March 25, 2003

CERTIFICATE OF MAILING OR TRANSMISSION

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner For Patents, Box ROE, Washington, DC 20231, or facsimile transmitted to the U.S. Patent and Trademark Office on the date shown below.		Address All Future Communication to: ARENT FOX KINTNER PLOTKIN & KAHN, PLLC 1050 Connecticut Avenue, N.W., Suite 400 Washington, DC 20036-5339
Name (Print Type)		
Signature		Date

Burden Hour Statement: This form is estimated to take 0.2 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND Fees and Completed Forms to the following address: Assistant Commissioner for Patents, Box RCE, Washington, DC 20231



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

#11/B
4/2/3
Sunder

In re Application of:

Confirmation No: 3840

Masaki KOMAKI

Art Unit: 2815

Serial No.: 09/939,752

Examiner: J. Nguyen

Filed: August 28, 2001

Docket No.: 024016-00014

For: FUNDAMENTAL CELL, SEMICONDUCTOR INTEGRATED
DEVICE, WIRING METHOD AND WIRING APPARATUS

PRELIMINARY AMENDMENT WITH FILING OF RCE

Commissioner for Patents
Washington, D.C. 20231

March 25, 2003

Dear Sir:

Prior to continued examination of the application, please amend the above-
identified application as follows:

IN THE CLAIMS:

Please amend and add the following claims:

B1
1. (Twice Amended) A fundamental cell, used as a basic unit in layout
of a semiconductor integrated circuit device, comprising:
no fixed wiring for commonly wiring between fundamental cells in a
hierarchy where fundamental cells are formed and
connector terminals to be connected to upper wiring layers.

B2
8. (Twice Amended) A semiconductor integrated circuit device,
comprising:
a fundamental cell, used as a basic unit in layout, having no fixed wiring to
be commonly wired between the basic units in a hierarchy where fundamental

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